Characterization of a 1-Pin Stress ESD Testing Method for the Analysis of Nanosecond-Range Charging Effects

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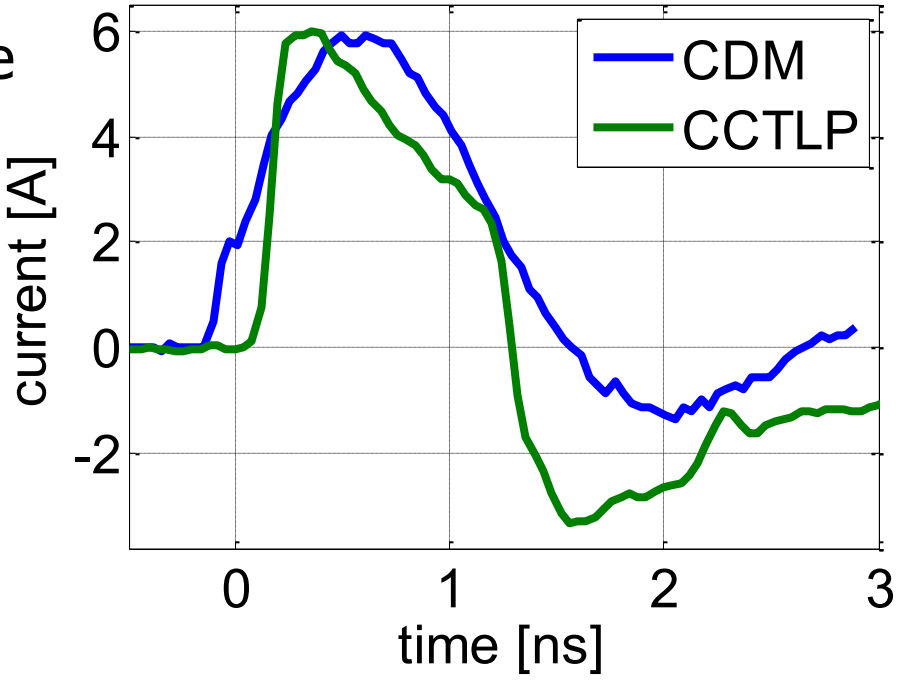
Objectives

- 1-pin ESD stress: Current flows all over the device
- **C**apacitively **C**oupled **T**ransmission **L**ine **P**ulse (**CCTLP**) offers advantages in comparison to **C**harged **D**evice **M**odel (**CDM**) test
- Advantages of CCTLP:
  - Measure current and voltage
  - Reproducibility (no spark)
  - Test on wafer and bare die
- Characterization and modeling of CCTLP test in order to simulate current and voltage (on chip)



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Outline

1 1-Pin ESD Stress

2 Device Parameters

3 Characterization

4 Simulation

5 Application

6 Conclusion

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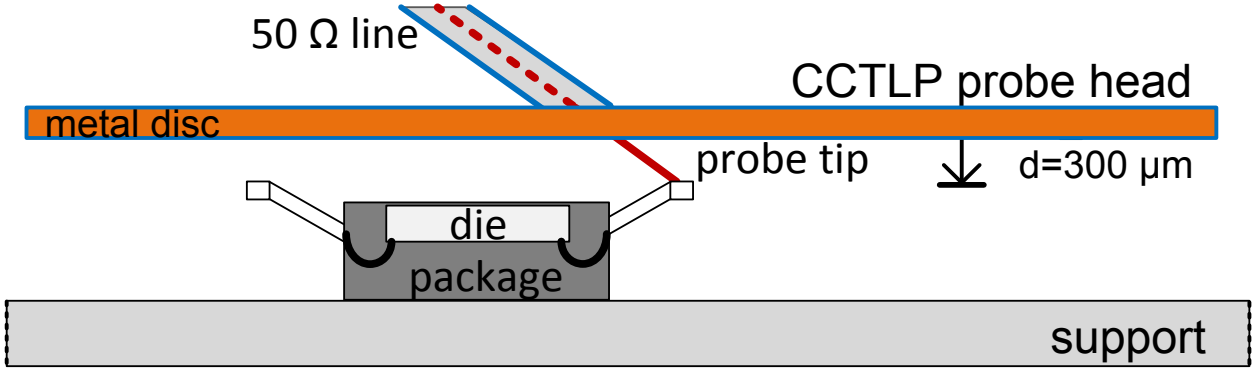
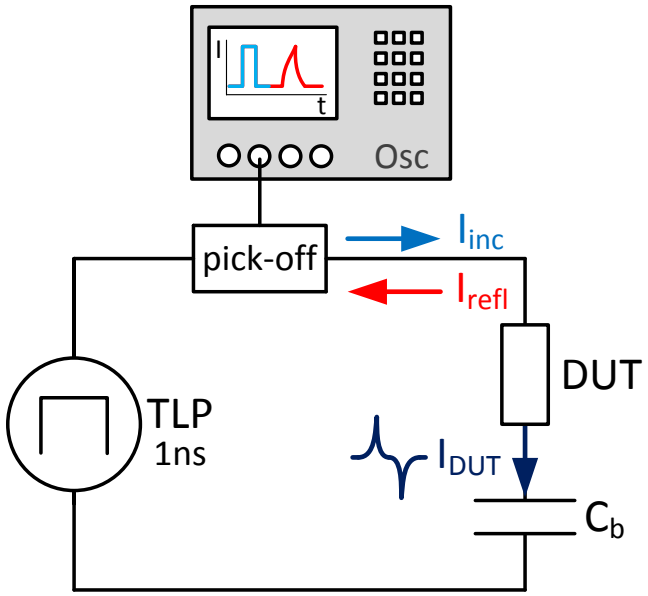
1-Pin ESD Stress: Setup

- CCTLP probe tip connects a single pin of a device
- Current return path is provided via metal disc Ø 50mm
- A **T**ransmission **L**ine **P**ulse (**TLP**) is used as excitation source (100ps rise time, 1ns pulse width)
- Current and voltage can be calculated from the incident and reflected waves





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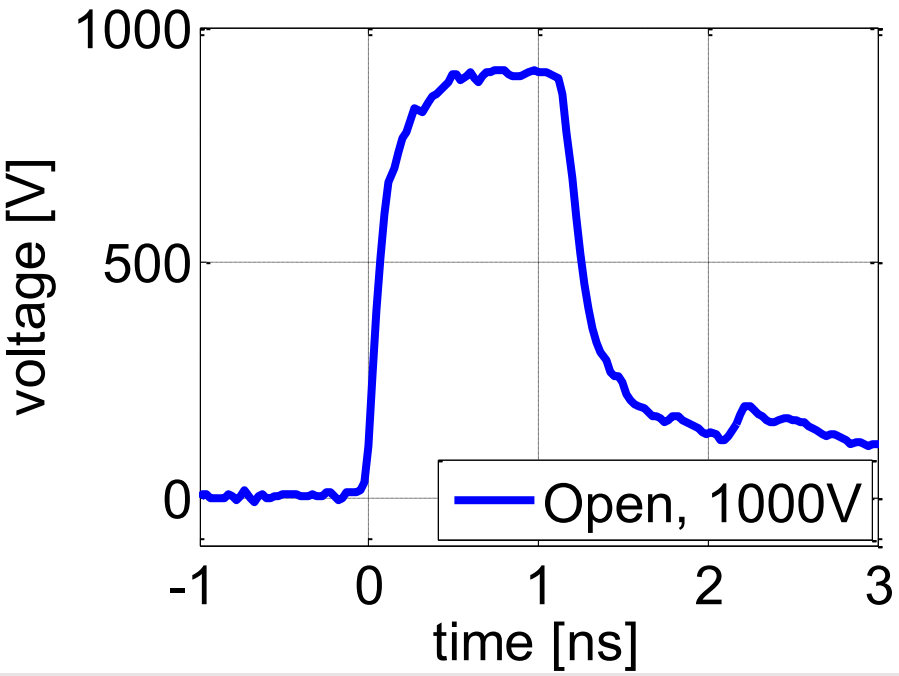
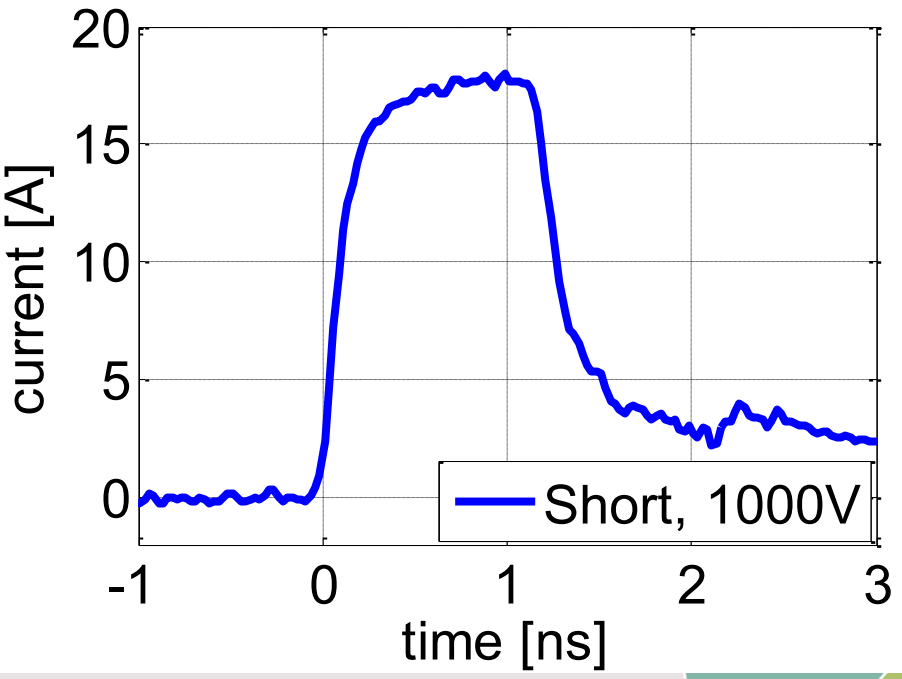
1-Pin ESD Stress: Losses

- Differences between voltage setting in the TLP software and measured values have to be quantified for the simulation setup
- Waveform verification by short and open measurement
- Overall 10% less voltage and current is measured





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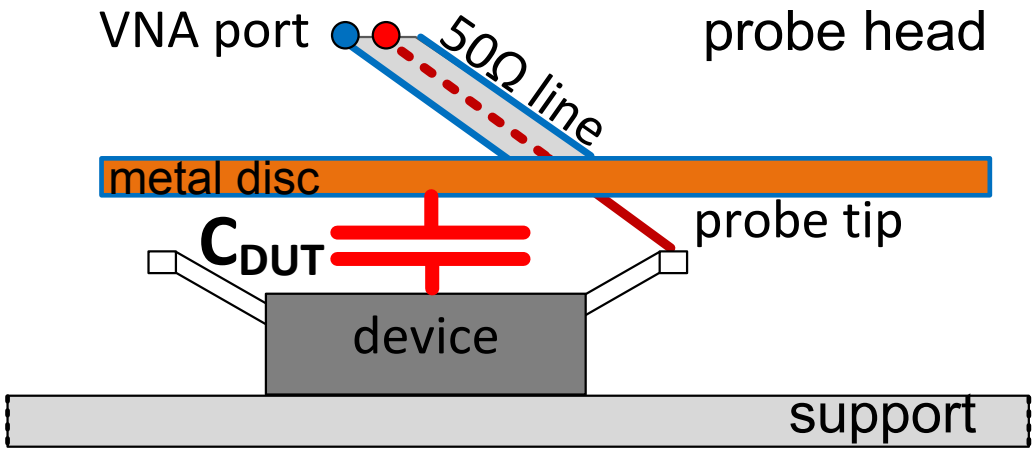
Device Parameters: Capacitance

- Current and voltage waveforms depend on the package and device capacitance C_{DUT}
- C_{DUT} can be measured with a network analyzer. The probe provides a 50Ω system up to the needle tip.
- Example devices:
  - Device A: Small sensor IC in QFN package
  - Device B: µC IC in LQFP package

Device	Pin	C_{DUT} [pF]
A	V_{SS}	3.4
	NC	0.3
B	V_{SS}	19.3
	Epad	17.0



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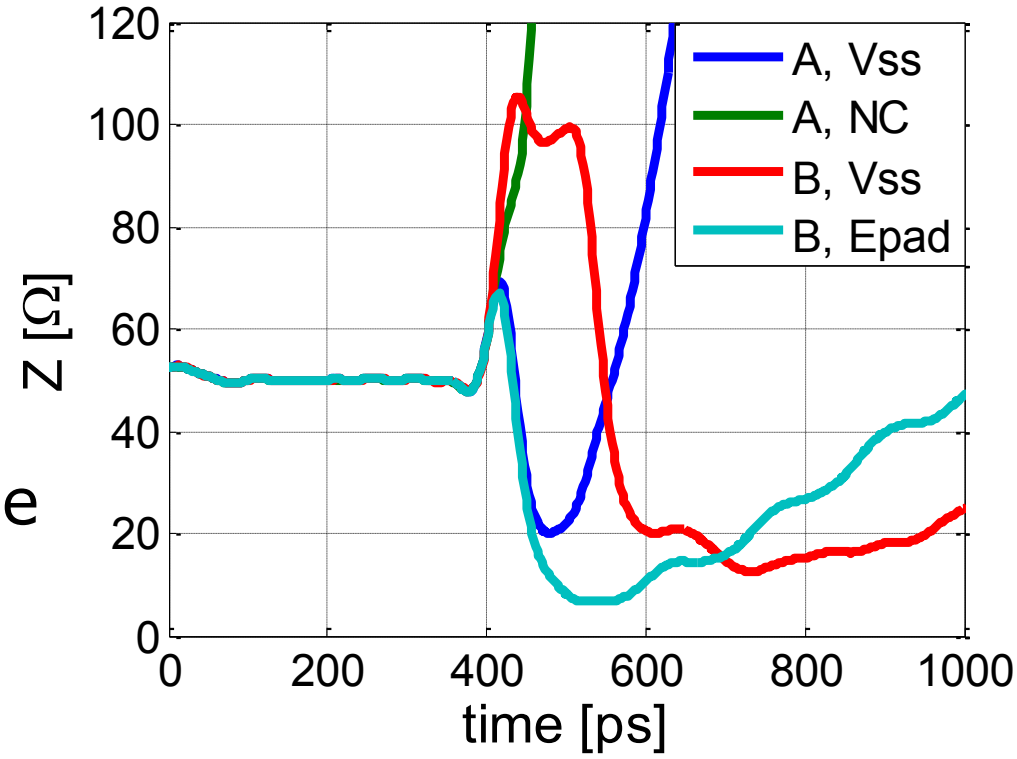
Device Parameters: Lead Frame & Bond Wires

- Lead frame and bond wire have an influence on waveforms
- Transmission path from pin to die can be measured with a TDR connected to the probe head:

- t < 400ps:
  - 50Ω line of CCTLP probe
- t > 500ps:
  - Dominated by C_{DUT}
- Device B, Vss: Leadframe
  - Z_{TL}=95Ω, t_{TL}=70ps



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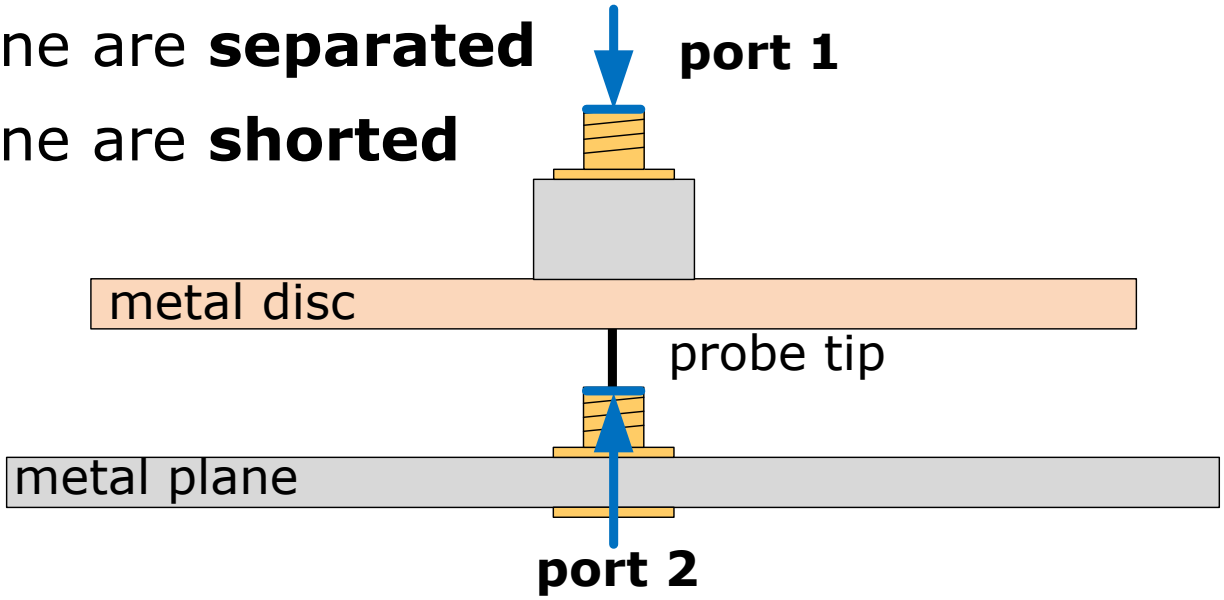
Characterization: Setup

- S-parameters are measured in a 2-port setup
  - Port 1: Excitation source -> TLP input
  - Port 2: Probe tip -> Contact to device
- Required bandwidth: 10GHz (TLP risetime 100ps)
- The probe is characterized in two ways:
  1. The disc and plane are **separated**
  2. The disc and plane are **shorted**



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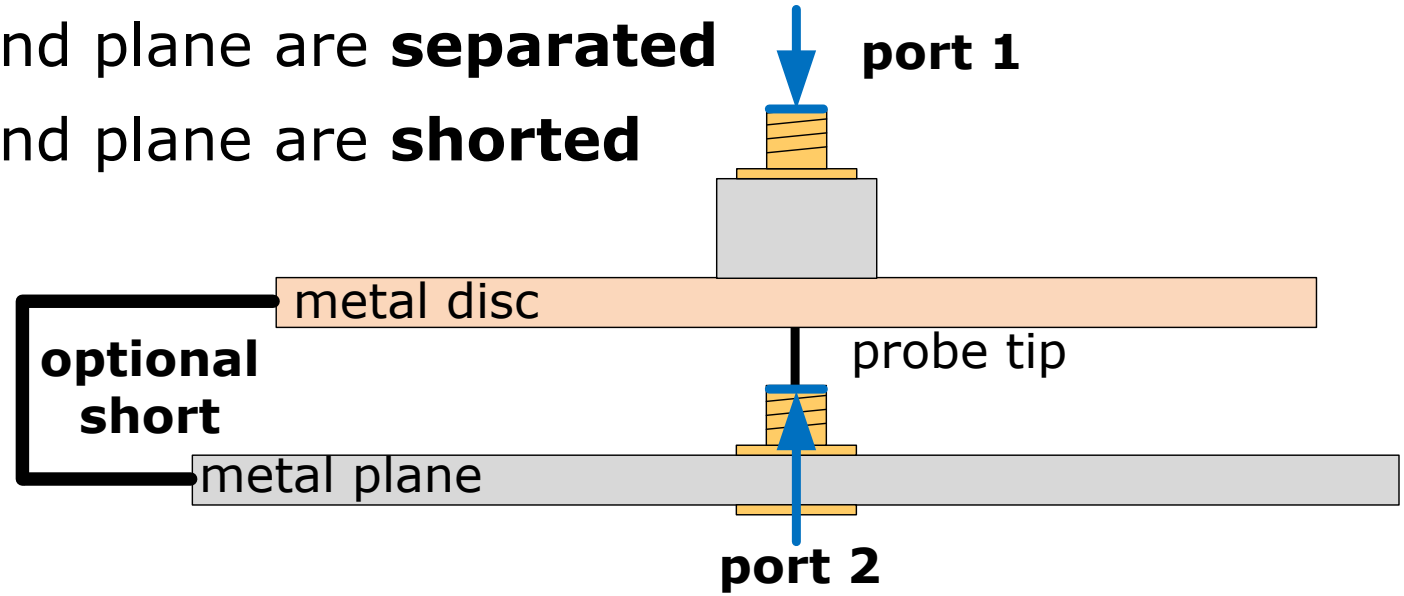
Resonances coming from GND system are suppressed



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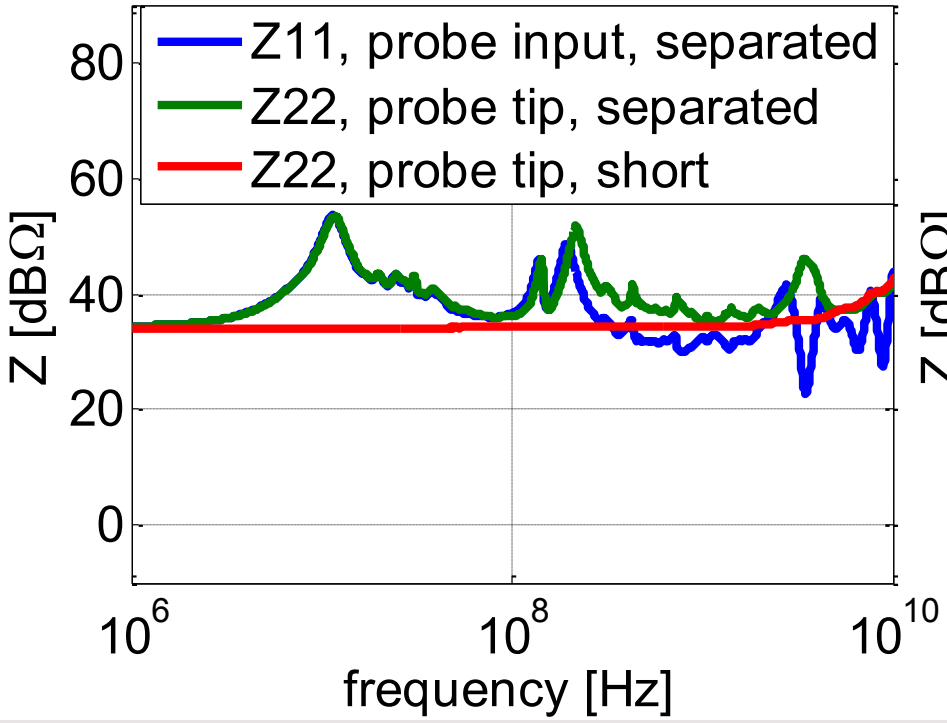
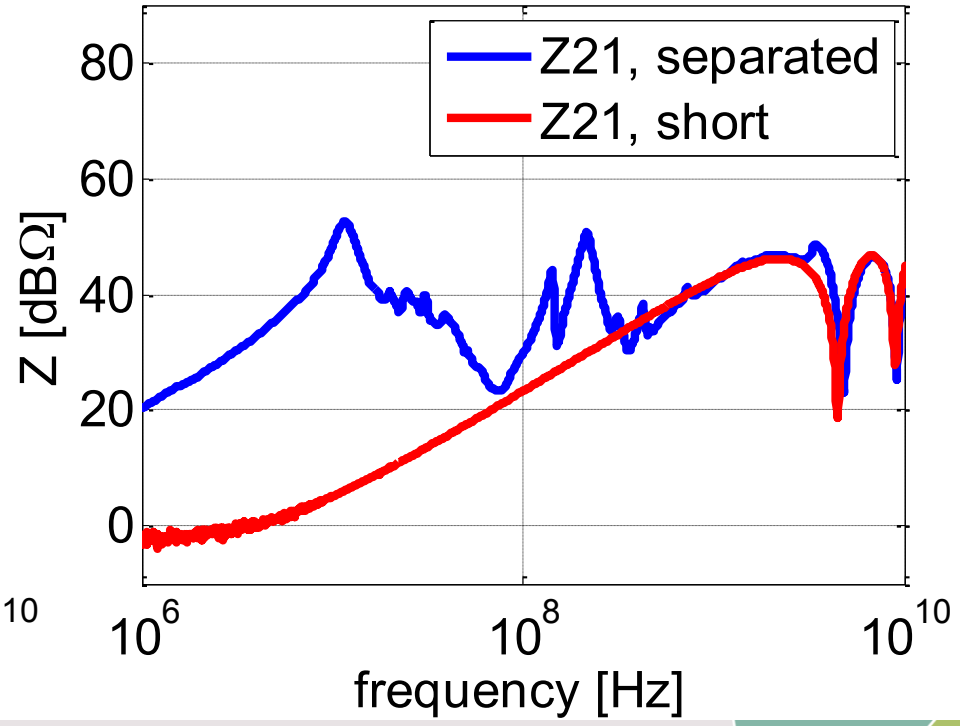
Characterization: Results

- Separated dataset shows resonances of current return path especially for frequencies up to 1GHz due to the 300µm gap
- Shorted dataset shows 50Ω up to several GHz





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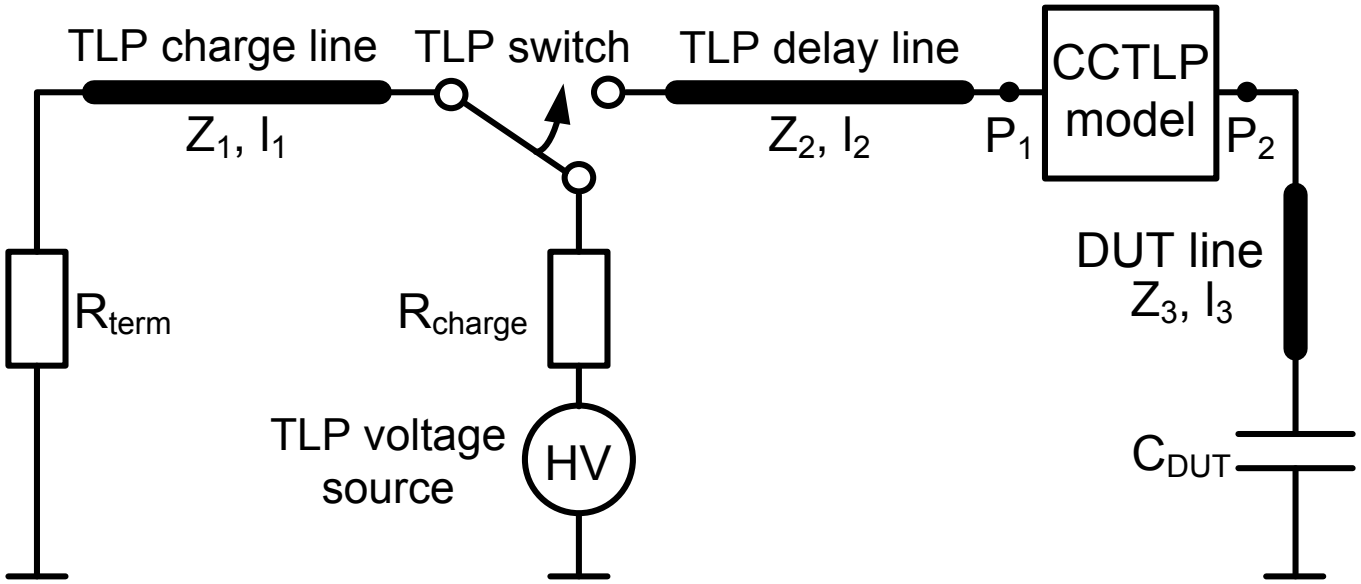
Simulation: Setup

- TLP-model: Two 50Ω transmission lines and switch
  - Charge line: 11cm or 26cm (1ns or 2.5ns pulse width)
- CCTLP-probe model: 2-port S-parameter dataset
- Device model: Capacitance C_{DUT}
  - Optional: DUT line for modeling extended packages



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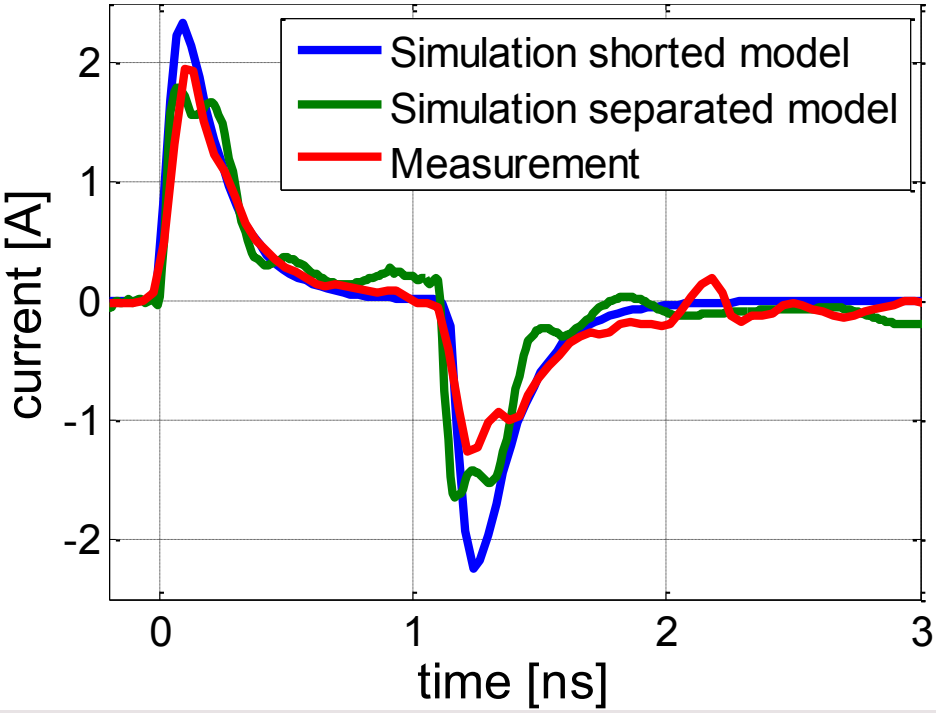
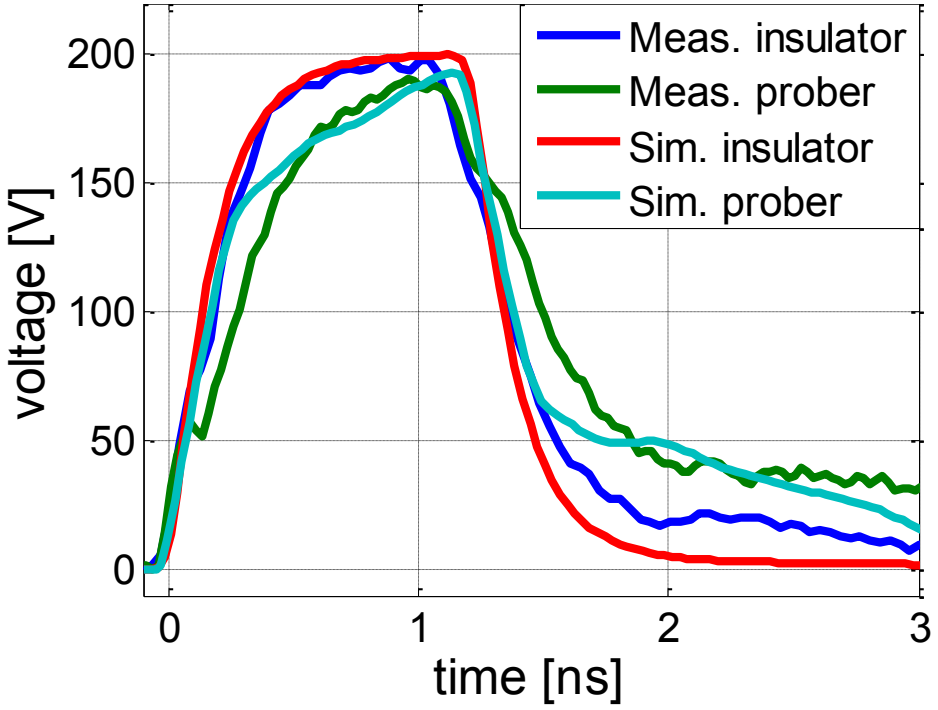
Simulation: Comparison of Models

- Comparison of measurement vs simulation (2 datasets)
  - Wafer prober vs. wooden table
- Example: Device A, V_{SS} (V_{TLP}=200V, C_{DUT}= 3.4pF)
- Waveform details are reproduced by "separated model"





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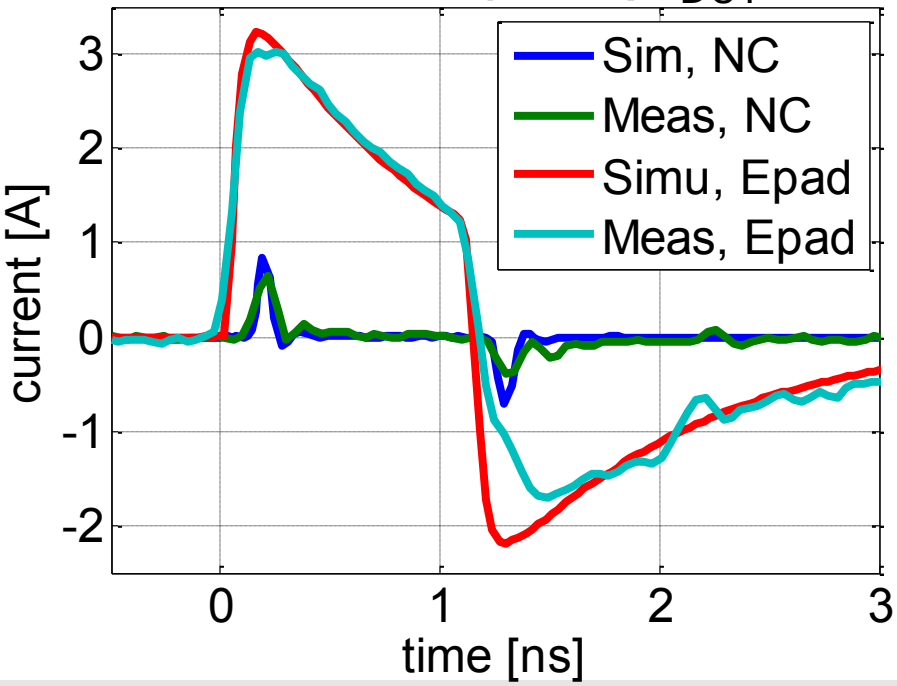
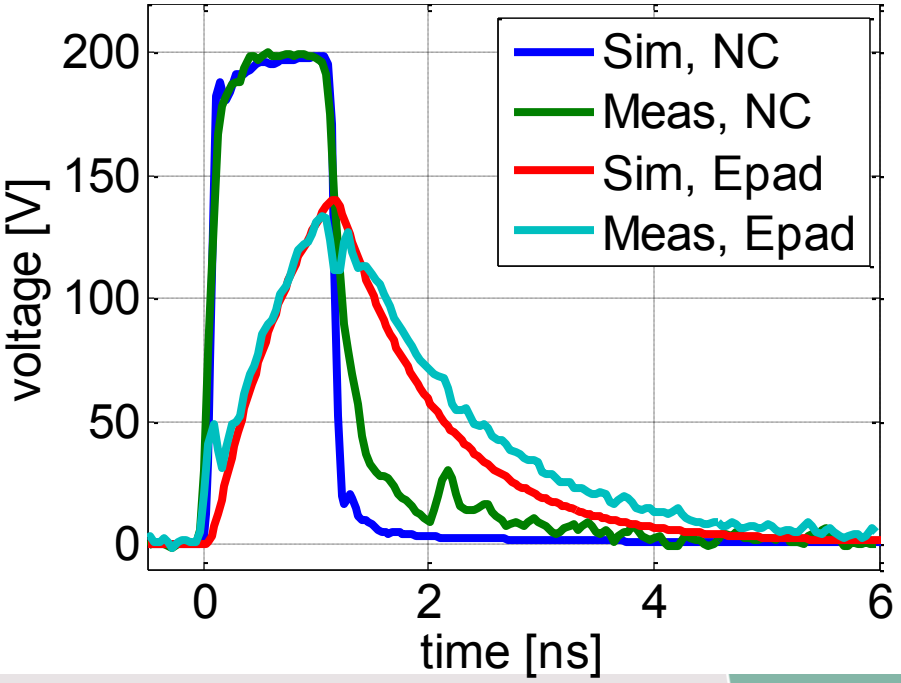
Application: Device Capacitance

- All waveforms are simulated using the shorted probe model. The device is placed on an insulating layer
- Simulation vs measurement for V_{TLP}=200V
  - Device A, NC (C_{DUT}= 300fF): Charging within 200ps
  - Device B, Epad (C_{DUT}= 17pF): V_{TLP} is not reached





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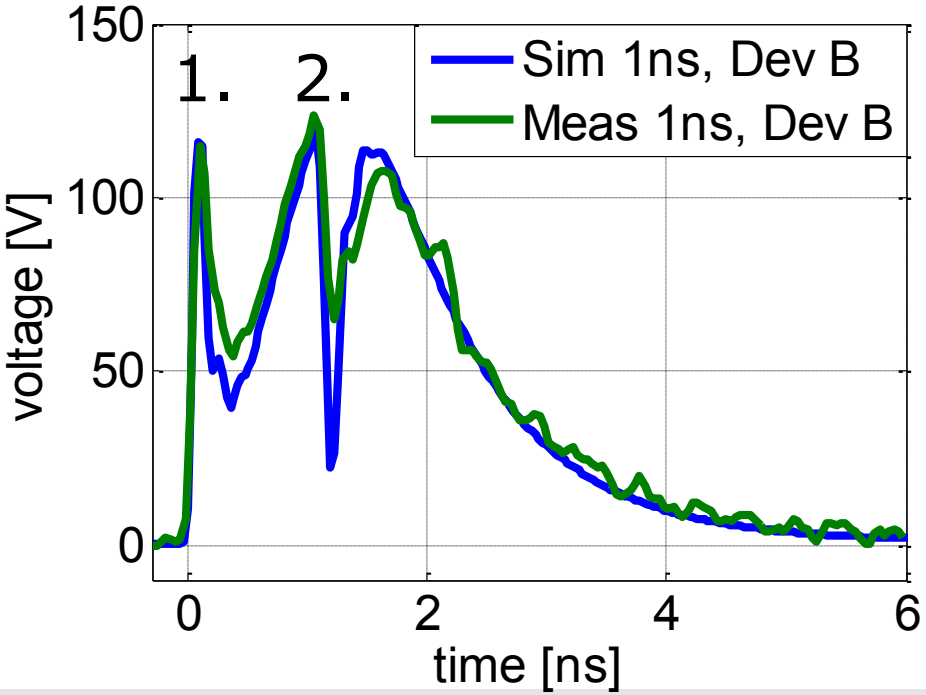
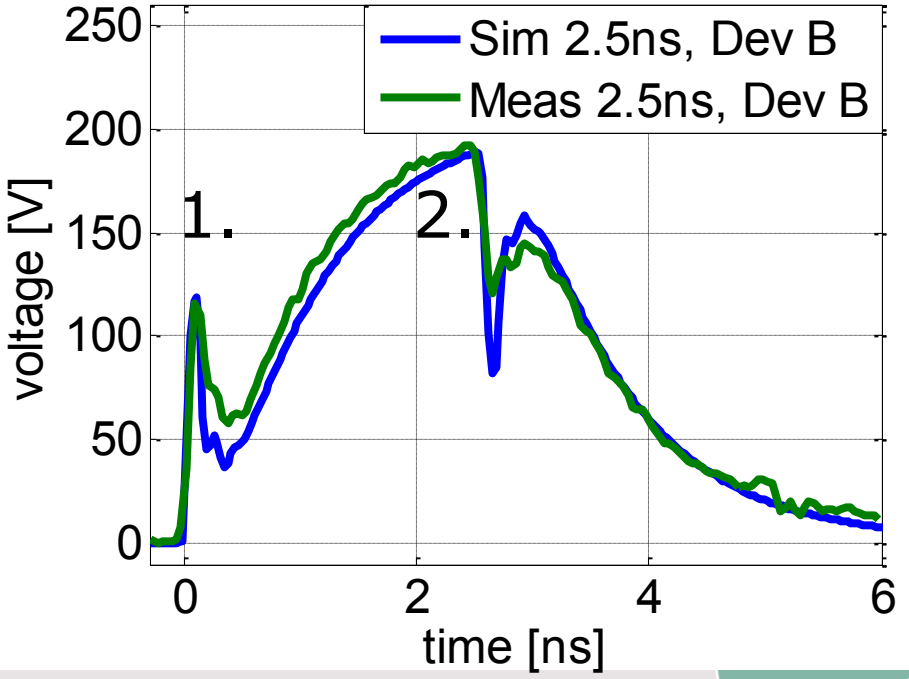
Application: Package and Pulse Width

- Example: Device B, V_{SS} (V_{TLP}=200V, C_{DUT}= 19.3pF)
  - Impedance Z_{TL}=95Ω, Delay t_{TL}=70ps
- The first peak is defined by path from pin to the die
- The second peak is dominated by device capacitance





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Conclusion

- Charging and discharging of semiconductor devices via a single pin is simulated using S-parameter models
  - Waveform shape is setup specific and can only be simulated exactly if characterization is done in the same setup as time domain stress.
- Advantages of the 1-terminal CCTLP-setup
  - Device capacitance can be measured with a VNA
  - Impedance and length of package traces are extracted with a TDR
- The simulation circuit can be extended by compact models of ESD structures in order to simulate the stress through a single device on silicon

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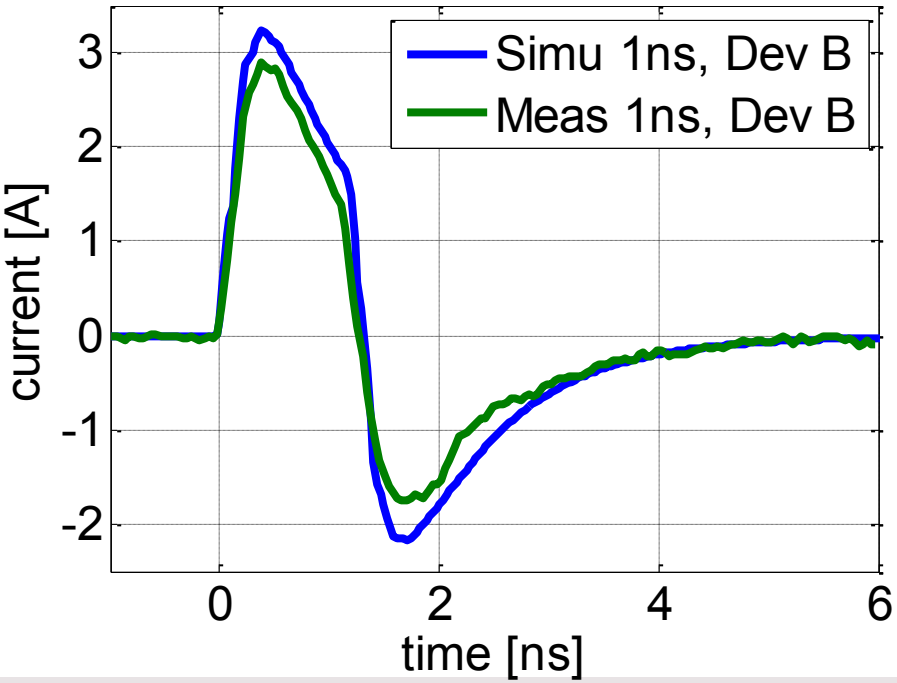
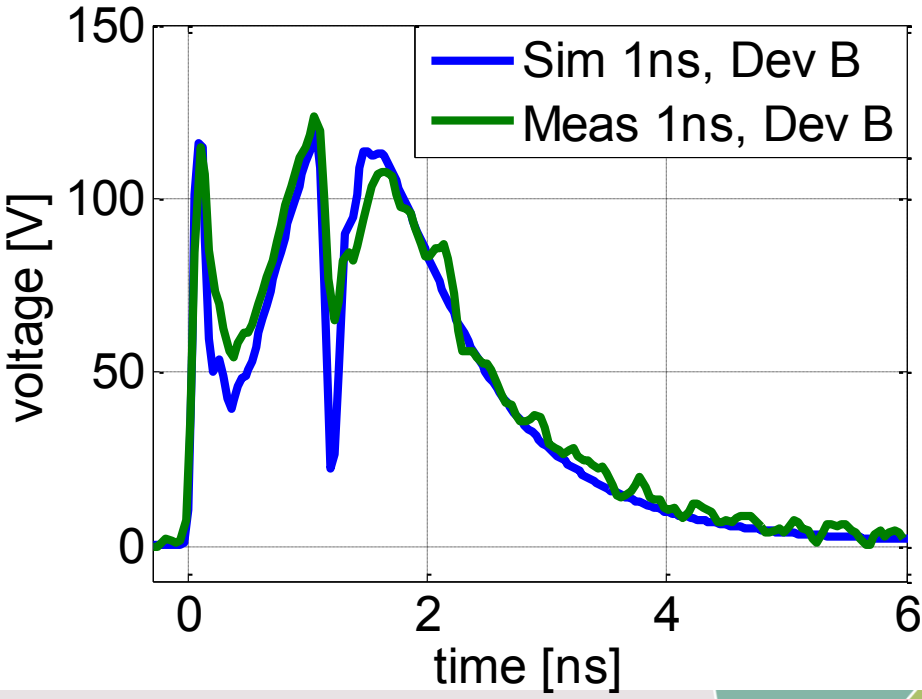
Appendix

- Comparison of current and voltage waveforms for the extended package
- Example: Device B, V_{SS} (V_{TLP}=200V, C_{DUT}= 19.3pF)
- Current waveform does not indicate package traces





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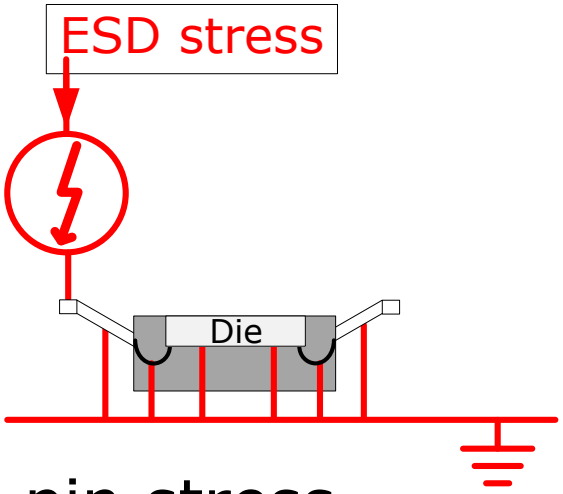
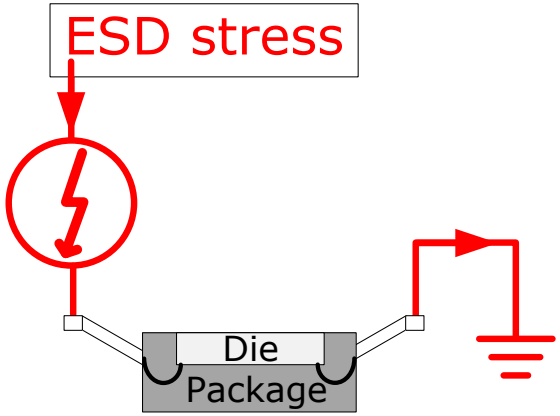
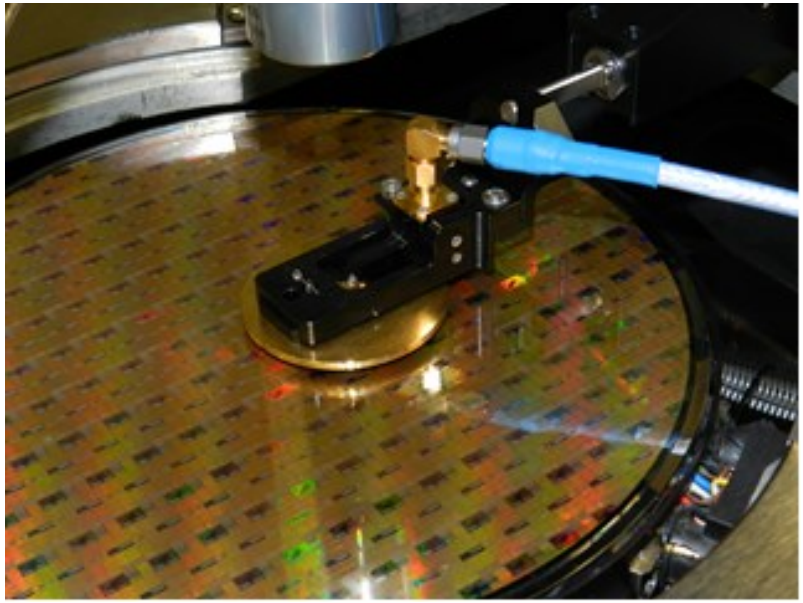
Appendix

- 1-pin stress



- 2-pin stress





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